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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,977	03/16/2004	Chris Smith	CD03005	3922

60909 7590 03/06/2009

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
03/06/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,977	SMITH ET AL.	
	Examiner	Art Unit	
	QUAN TRA	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 1/21/09. New grounds of rejection are introduced as necessitated by amendment.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The original specification fails to teach "components of said first circuit are placed in a fixed state during manufacturing", recited in claim 3. There is no word "manufacturing" found in page 10, line 22 to page 11, line 10.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara et al (USP 5994937) in view of Kwon (USP 5926045), Mitsuishi (USP 6031366) and Saeki (USP 6388490).

As to claims 1 and 4, Hara et al.'s figure 4 shows a timer circuit comprising an output stage (404) coupled to a configurable delay element (402); and a pull-down path (414) coupled

to the output stage, the pull-down path coupled to receive a reference signal (Vref) that varies in proportion to temperature (figure 5) and wherein a delay through the timer circuit is inversely proportional to the temperature. The full down path functions as current source. Thus, figure 4 shows all limitations of claim 1 except for the pull-down path is a variable current source. However, Kwon's figure 2 shows a timer circuit having variable current source 20 coupled to output state 10 for adjusting the slew rate or frequency outputted from the output state 10. Therefore, it would have been obvious to one having ordinary skill in the art to make Hara et al.'s pull-down path to be a variable current source for the purpose of having more flexibility of controlling output slew rate. The modified Hara et al.'s figure 4 fails to show the detail of the modified current source (414). However, Mitsushi's figure 3 shows a variable current source that compatible with Hara et al.'s pull-down state and having simple structure. Therefore, it would have been obvious to one having ordinary skill in the art to use Mitsushi's variable current source for Hara et al.'s modified current source (transistor 424) for the purpose of saving cost. The further modified Hara et al.'s fails to show plurality of selectively active component that comprises a plurality of gated capacitors which can be selectively coupled to the output stage via a plurality of corresponding pass gates. However, Saeki's figure 3 shows a plurality of gated capacitors (CAP11-CAP15) which can be selectively coupled to output stage MP01-MN02 via a plurality of corresponding pass gates MN11-MN15 in order to adjust the delay outputted from the output stage. Therefore, it would have been obvious to one having ordinary skill in the art to add Saeki's delay adjusting circuit to Hara et al.'s delay stage for the purpose of having more flexibility of controlling the delay of the signal outputted by the delay stage. Thus, the modified Hara et al. reference shows that the pull down path (the modified 414) comprising first circuit (Mitsuishi's figure 3) for provide selectable amount of pull down current, wherein the first circuit comprises plurality of individual configured components (Matsuishi's IS1-ISn); and shows

plurality of selectively-activated components (Saeki's capacitors) that comprise components (capacitors) which are of different from components type (capacitors) than the plurality of individual-configured components (Mitsuishi's transistors), the pulldown path further comprising a second circuit (circuit that generates Vref) for varying the delay through the timer circuit base upon temperature, wherein the second circuit is operable to vary the delay based upon a reference signal (Mithsuishi's VB or Hara et al.'s Vref), and wherein the delay is inversely proportional to temperature.

As to claim 2, the modified Hara et al.'s figure 4 shows that the reference signal is derived from a band gap reference circuit (figure 5).

As to claim 3, one skilled in the art would have realized that during manufacturing, there is no power supply and signal input to the circuit. Therefore, plurality of individual-configured components of the first circuit are placed in a fixed state during manufacturing.

As to claim 6, the modified Hara et al.'s figure 4 shows that the plurality of individual-configured components comprise a plurality of gated pull-down circuits coupled in parallel wherein each gated pull-down circuit comprises a first switch (Sn) having controlled by a respective configuration bit and a series coupled second transistor (Mn) having a gate controlled by said reference signal. The modified Hara et al.'s figure 4 fails to shows that the switches S1-Sn are transistors. However, transistor using as a switch is well known in the art. It would have been obvious to one having ordinary skill in the art to use transistors for switches S1-Sn for the purpose of saving space and cost.

Claims 10 and 11 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claims 15 and 16, it is seen as an intended use for using the modified Hara et al.'s in a memory circuit.

As to claim 5, the modified Hara et al.'s figure 4 shows that the configurable delay element further comprises a plurality of configuration bits (inputs of Saeki's transistors MN11-MN15) each for controlling a respective pass gate.

As to claim 7, the modified Hara et al.'s figure 4 shows that the plurality of individual-configured components comprise a plurality of gated pull-down circuits coupled in parallel wherein each gated pull-down circuit comprises a first switch (Sn) having controlled by a respective configuration bit and a series coupled second transistor (Mn) having a gate controlled by said reference signal. The modified Hara et al.'s figure 4 fails to shows that the switches S1-Sn are transistors. However, transistor using as a switch is well known in the art. It would have been obvious to one having ordinary skill in the art to use transistors for switches S1-Sn for the purpose of saving space and cost.

As to claim 8, the modified Hara et al.'s figure 4 shows that the plurality of selectively activated components comprises a plurality of gated capacitors which can be selectively coupled to the output stage via a plurality of corresponding pass gates.

As to claim 9, the modified Hara et al.'s figure 4 shows that the configurable delay element further comprises a plurality of configuration bits each for controlling a respective pass gate.

Claims 12-14 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claim 17, the modified Hara et al.'s figure 4 shows a method of varying a delay of a timer circuit comprising: during configuration of the timer circuit (time that the variable current source and variable capacitor are varied), setting a first plurality of configuration bits (signals that control the newly added capacitors) which control the amount of elements coupled to an output stage of the timer circuit to set an amount of delay through the timer circuit; during the

configuration, setting a second plurality of configuration bits (signal that controlling the variable current source) which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through the timer circuit, the pull down path coupled to the output stage, wherein said pull down path comprises a plurality of individually-configured components (Mitsuishi's IS1-ISn in the modified 414), and wherein each of said plurality of individually-configured components corresponds to a respective configuration bit of said plurality of configuration bits; and during operation of the timer circuit (other period different from the configuration period), varying the delay of the timer circuit in response to a varying of a reference signal (Vref is varied when temperature varies), wherein the delay of the timer circuit comprises is inversely proportional to temperature (the reference voltage is proportional to absolute temperature, thus, as temperature increases, the reference voltage is increased. More pull down current is generated. Thus, less delay is provided).

Claims 18-20 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN TRA whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/QUAN TRA/
Primary Examiner, Art Unit 2816